Remarks

In the present response, no claims are amended. Claims 1 – 23 are presented for examination.

I. **Claim Rejections: 35 USC § 103**

Claims 1-4, 6, 11-15, and 17 are rejected under 35 USC § 103 as being unpatentable over USPN 6,101,577 (Tran) in view of USPN 5,371,877 (Drako). This rejection is traversed.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. Applicants assert that the rejection does not satisfy these criteria.

No Suggestion/Motivation to Modify/Combine References

For at least the following reasons, no suggestion or motivation exists to modify or combine Tran in view of Drako.

First, Applicants argue that no teaching or suggestion exists to make the combination because the references are directed to completely different inventions. Tran is directed to a microprocessor having an instruction cache with access times greater than the clock cycle time of the microprocessor (3: 26-30). In order to increase fetch bandwidth, the instruction cache "is configured into banks which can be separately accessed in a pipelined fashion (i.e., a second instruction block fetch is initiated prior to completing a first instruction block fetch)" (5: 51-56). **By contrast, Drako teaches a completely different invention.** Drako teaches a single port random access memory to perform the function of a conventional dual port FIFO memory (1: 48-50). In FIG. 2 (the primary embodiment of Drako's invention), Drako shows how a single port random access memory is used to provide dual port FIFO memory that both receives and furnishes data (3: 61-64).

PAGE 8/12 * RCVD AT 4/6/2006 4:17:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:281 514 8332 * DURATION (mm-ss):03-04

The Examiner must provide *objective evidence*, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Such teaching or suggestion does not exist.

Second, Applicants argue that no teaching or suggestion exists to make the combination because the references are directed to solving completely different problems. In Tran, the Background section discusses numerous problems associated with cache access time. "Unfortunately, increasing the size of the caches generally creates a greater cache access time" (2: 52-53). **By contrast, Drako solves completely different problems.** In Drako, the Background section discusses that traditional dual ported FIFO memory is quite expensive when compared with single port memory (1: 33-35). As another problem, this dual ported memory requires additional circuitry and thus increases the overall size of the circuitry (1: 40-45).

To establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

In light of the completely different inventions and problems being solved in Tran and Drako, no suggestion or motivation exists to combine or modify these references.

For at least these reasons, Applicant respectfully asks the Examiner to withdraw the rejection since a *prima facie* case of obvious has not been established.

Response to Examiner's Arguments on Combination

The Examiner argues that the combination of Tran and Drako are obvious because Drako provides Tran with reduced memory hardware and such combination could be readily accomplished. Applicants respectfully disagree.

PAGE 9/12 * RCVD AT 4/6/2006 4:17:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:281 514 8332 * DURATION (mm-ss):03-04

As discussed above, Tran and Drako are directed to different inventions that solve different problems in the art. No motivation exists to combine these references. Instead, the Examiner is performing an improper piecemeal construction that uses hindsight to arrive at the claim elements. In other words, the Examiner is picking and choosing sentences or teachings from Tran and Drako with hindsight of Applicants' invention to allegedly obviate the pending claims. One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

No Reasonable Expectation of Success

No reasonable expectation of success has been established for modifying Tran with the teachings of Drako to arrive at the recitations of the claims. In other words, even assuming *arguendo* that Tran and Drako are combinable (which they are not), the combination will not yield a reasonable expectation of success.

Figure 4 in Tran expressly teaches a cache architecture having dual ported memory banks. Figure 2 in Drako teaches quite complex dual ported FIFO memory that both receives and provides data simultaneously utilizing conventional singe port random access memory (2: 6-9). The complex arrangement in Drako's Figure 2 cannot simply be fit into or substituted in the cache architecutre of Tran's Figure 4. **This substitution or exchange simply will not work.** Drako teaches that many inverter circuits, AND gates, multiplexors, clocks, synchronizations between various circuits, etc. must be coupled to the single ported RAM devices. One skilled in the art knows that the complex architecture disclosed in Drako cannot be substituted into the instruction cache architecture of Tran.

In view of these deficiencies, the Office Action has failed to establish a reasonable expectation of success with a combination or modification of Tran and Drako. Therefore, the *prima facie* case of obviousness has not been established.

All Elements Not Taught or Suggested

All of the elements of the claims are not taught or suggested in Tran and Drako. In other words, evening assuming *arguendo* that Tran and Drako are successfully

PAGE 10/12 * RCVD AT 4/6/2006 4:17:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:281 514 8332 * DURATION (mm-ss):03-04

combinable (which they are not), the alleged combination does not teach or suggest all the elements in the claims.

Independent claims 1 and 12 recite a processor having a branch predictor with a multi-bank prediction array. **Each of these banks comprises a single-ported memory device.** The combination of Tran and Drako does not teach or suggest this recitation.

The Examiner admits that Tran does not teach a branch predictor having memory banks as a single-ported memory (see OA at p. 4). Applicants agree with this admission. The Examiner, however, attempts to cure this deficiency with Drako. Applicants respectfully disagree.

In light of the Examiner's admission, the issue is: Does Drako teach or suggest a branch predictor with a multi-bank prediction array wherein each of the banks is a single-ported memory device? Drako does not. First, Drako does not even discuss or even suggest branch predictors whatsoever. Further, nowhere does Drako teach or suggest multi-bank prediction arrays. Again, Drako is completely silent on processor prediction and multi-bank arrays for branch prediction.

Independent claims 1 and 12 explicitly recite that the banks of a multi-bank prediction array comprise a single-ported memory device. Figure 2 of Drako does teach a complex circuit that uses two single port RAMs. These memories, however, are not part of a multi-bank prediction array that is used for predictions for conditional branch instructions.

For at least these reasons, independent claims 1 and 12 and their dependent claims are allowable over Tran in view of Drako.

II. Allowable Subject Matter

Applicants sincerely thank the Examiner for indicating allowance of claims 5, 7-10, 16, and 18-23.

PAGE 11/12 * RCVD AT 4/6/2006 4:17:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:281 514 8332 * DURATION (mm-ss):03-04

CONCLUSION

In view of the above, Applicants believe that all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. (832) 236-5529. In addition, all correspondence should continue to be directed to the following address:

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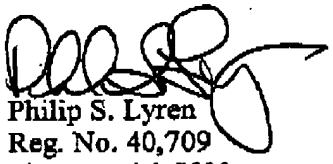
Respectfully submitted,



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CERTIFICATE UNDER 37 C.F.R. 1.8

The undersigned hereby certifies that this paper or papers, as described herein, is being transmitted to the United States Patent and Trademark Office facsimile number 571-273-8300 on this 6th day of April, 2006.

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PAGE 12/12 * RCVD AT 4/6/2006 4:17:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:281 514 8332 * DURATION (mm-ss):03-04